A new paradigm for in-line detection and control of patterning defects

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ABSTRACT

With continuously shrinking design rules and corresponding low-k1 lithography, defectivity and yield are increasingly dominated by systematic patterning defects. The size of these yield-limiting defects is shrinking along with feature size, making their detection and verification more difficult. We discuss a novel, holistic approach to pattern defect detection and control, which integrates full chip layout analysis and hybrid wafer metrology data to predict wafer locations with highest probability for defect occurrence. We assess the various components of this flow by an experimental study on a 10 nm BEOL process at IMEC, using state-of-the-art negative tone development (NTD) and triple Litho-Etch patterning process.

Keywords: patterning defect, hotspot monitoring, holistic lithography, 10 nm, design hotspots, process window, defect prediction, defect verification, defect control

1. INTRODUCTION & CONCEPT

It is widely recognized that continuing semiconductor node scaling keeps pushing tighter requirements in all aspects of patterning process control. Shrinking feature sizes generally imply diminishing margins for imaging and overlay and higher sensitivity to process variations. Reticle enhancement technologies using computational lithography, i.e. litho-model based optimization, have been developed to maintain the best possible process window (PW) entitlement for device patterns; nevertheless, there is a diminishing gap between process margins and traditional control capabilities.

Another development is that device yield, which historically was limited primarily by random defects, has become more and more susceptible to design-layout related patterning defects, in particular for back end of the line (BEOL) layers.[1] Overall process window of a device layout may be limited by particularly sensitive critical pattern geometries, i.e. hotspots. This poses a challenge for process monitoring, if the latter is performed by metrology on test structures that may not fully represent the sensitivities of device patterns. In addition, detecting defects by optical inspection tools has become more challenging due to the reduction of critical defect sizes that follow the shrink of pattern geometries.

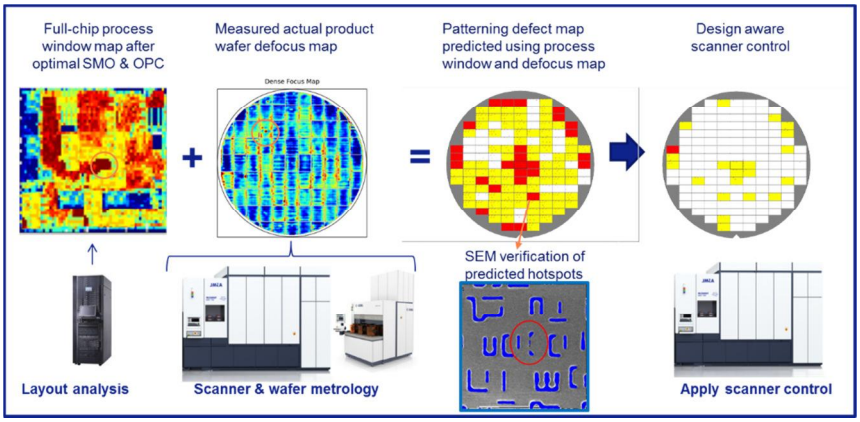

Figure 1: Holistic lithography concept for patterning defect prediction, defect verification and layout aware scanner control

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Holistic lithography optimization was introduced as a framework to improve on-product performance by close integration of litho tool operation, on-product wafer metrology and computational lithography. As detailed in Ref. 2 [Mulkens], the corresponding system architecture for in-fab optimization comprises scanner control interfaces, inline and standalone wafer metrology using scatterometry tools[3], and a computation and data management platform. Computational lithography components are also part of the solution, including source mask optimization (SMO), process-window aware and other advanced optical proximity correction (OPC), and full-chip layout verification. These are primarily being applied before or during final mask layout generation, although model-based approaches have also been introduced for scanner tuning to improve tool matching or control of lens-heating effects.[4-6]

The two key extensions from the existing framework are 1) a closer integration of the computational lithography component, for the purpose of reticle layout analysis, and 2) larger utilization of scanner metrology data, in particular topography and focus related data from the tool's leveling system.

The scanner metrology data will be combined with in-line scatterometry measurements of focus-indicating metrology targets[3], to construct a dense map of estimated focus variations across an entire wafer. Since the topology of each wafer is recorded by the scanner's leveling system, this map can be constructed for every single wafer being processed.

The output of the layout analysis should provide a sufficiently accurate representation of any specific reticle layout in terms of local process window boundaries, as well as a map of the most critical and PW limiting pattern locations. By combining the information on intra-field available process margins with the estimated process variations, here in particular the dense focus map, a defect prediction model can highlight locations which have the highest probabilities of layout hotspots becoming actual printing defects. These defect predictions results will drive efficient on-product wafer monitoring, verification and finally algorithms that optimize scanner operation in a most yield-relevant way.

In the remainder of the paper we will concentrate on experimental assessments of focus mapping as well as defect prediction and verification aspects. Future work will address extensions of the concept to include additional parameters, data sources, and control capabilities, such as reticle and process fingerprints, dose control etc.

2. TEST CASE & EXPERIMENTAL APPROACH

The experimental work to establish feasibility of defect prediction and verification was carried out at IMEC, using their 10 nm node BEOL DUV immersion process and test vehicle, which are described in Ref 7. [Vandewalle] The source was optimized extensively by SMO, and PW-aware OPC was used to generate the final mask layout. A full-chip mask set was constructed from a set of standard cells being combined in a pseudo-random configuration that places the same pattern in a multitude of different local environments. The layout covers half of the available scanner exposure field, i.e. 26 mm x 16 mm with several large areas of logic and SRAM designs.

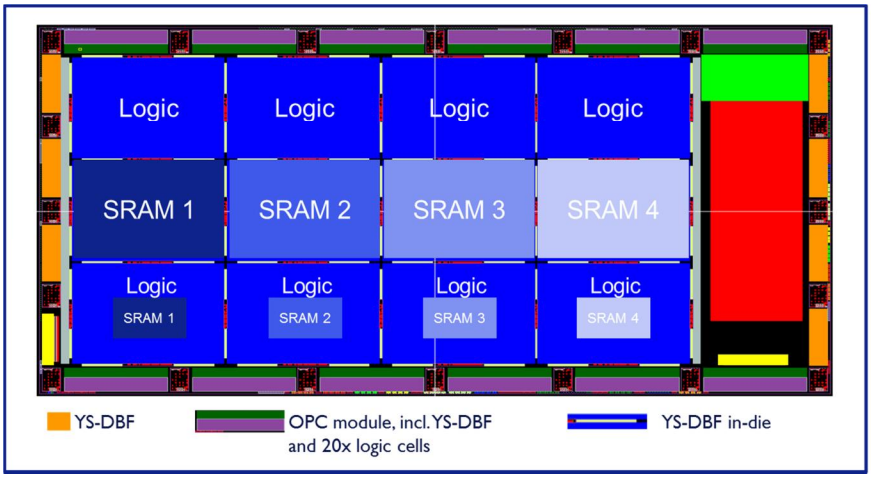

Figure 2a: IMEC SN2 mask layout.

Some smaller logic clips (40x40um^2) were placed at 12 locations with the same clip locally repeated 20 times to enable characterizations of local process variations and signal-to-noise ratios. In addition, a large number of monitoring modules with scatterometry targets and OPC model calibration structures were placed in the reticles. These include a large number of Diffraction Based Focus (DBF) metrology targets placed throughout the exposure field to enable validation of the dense focus map generation. The test vehicle is labeled Supernova2 or SN2. An overview of the reticle layout is shown in Fig.2a.

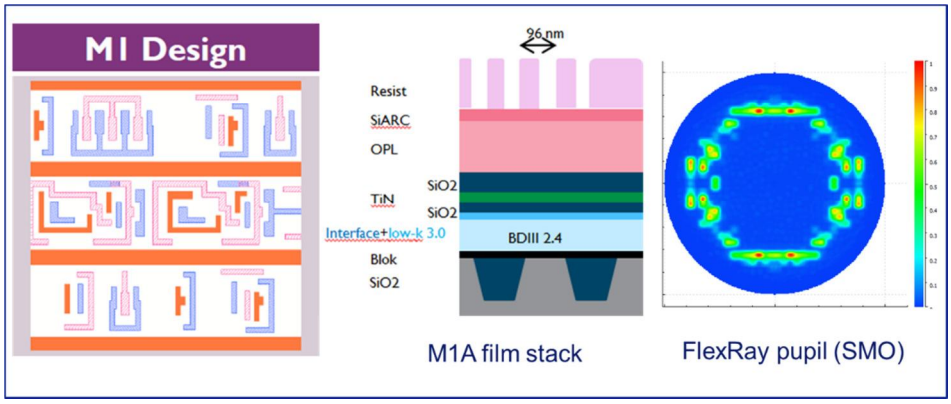

Figure 2b: Details of IMEC's M1 immersion DUV process.

We use Tachyon LMC (Lithography Manufacturability Check) and a well calibrated Tachyon FEM+ model[8] [Hunsche] for full-chip layout analysis, process window prediction and identification of most critical device patterns. As the test mask layout is constructed from repetitive placement of a limited number of similar unit cells throughout almost the entire mask area, we do not see any long-range spatial variation of local PW or layout-related best focus shifts, which may be present in more complex device layouts.

For the experiments we primarily use a single exposure of the M1 layer, which is per se defined as a triple patterning (LELELE) process, using 1.35NA and FlexRay freeform illumination, as illustrated in Fig. 2b. The resist process uses state of the art Negative Tone Development (NTD). All wafer exposures are on a 9-layer film stack that will support full LELELE processing, although there is no under-layer patterning and therefore no significant product specific, or process dependent, wafer topography.

All wafer exposures are done on a NXT:1950i immersion scanner. For each wafer we need to know the local variation as seen by the lithography tool, which has scanner-specific artifacts related to wafer chuck, leveling sensor, leveling correction, lens system, immersion and exposure process, etc. For each exposed wafer we collect detailed focus related data on the scanner, primarily from three data sources: 1) from the leveling system, which maps the topography of every wafer as mounted on the chuck before exposure; 2) from dynamics tracing of the servo performance, i.e. wafer and reticle stage positioning; 3) from the lens model which continuously predicts aberration state of the projection lens, which determines a lens fingerprint contribution to the total focus variations.

We also obtain focus measurements in resist, after wafer exposure and develop, using a YieldStar angle-resolved scatterometry tool and DBF targets.[9] These are line-space patterns with deliberate asymmetry that is introduced by one-sided application of sub-resolution features. A resulting asymmetry in printed resist profiles is detected on YieldStar by differential measurement between the positive and negative first diffraction orders. The asymmetry signal is almost linearly dependent on focus, whereas other, process related variations primarily affect the symmetrical 0th order signal. Several DBF target designs were included in the reticle layouts, in scribe lines between the large device blocks as shown in Fig. 2b. After characterization of the DBF performance, the best performing target design is chosen for focus monitoring.

For defect verification we rely primarily on SEM imaging tools. Most of the data presented here is generated at IMEC with a review SEM (KLA Tencor, edr7100), which provides relatively easy addressing for image acquisition at arbitrary locations on the wafer. We also consider usage of CD-SEM (Hitachi CG 5000) and e-beam inspection tools,as discussed

below, which each offer some unique characteristics and analysis capabilities. We also executed several PWQ-like (process window qualification) experiments using a bright field wafer inspection tool (KLA 2835) and subsequent SEM review, to check for the possibility of defect types that might be missed by the model based approach. All experimental data is from measurements in resist after develop, i.e. ADI.

3. RESULTS & DISCUSSION

3.1 Dense focus map generation and validation

The number of DBF target locations that we included in the SN2 reticle (~100) is an order of magnitude larger than what would typically be made available on product reticles. With the data from the latter, focus offsets and tilts with respective to the x and y axes (Rx, Ry, respectively) per exposure field may be determined by linear fitting. In order to construct a 'hybrid' dense focus map (HDFM), the low-spatial frequency DBF data will be combined with the complementary, much denser sampled scanner contribution. Figure 3 shows one example of HDFM generated for one of the wafers used in our experiments. The DBF data for HDFM generation are based on a sub-sample of 12 target locations within each exposure field, which are corrected and smoothly interpolated to determine the general focus shape. The scanner contribution is available on the sampling grid of the leveling sensor, which has 9 measurement spots along the slit direction and generates topography measurements at roughly every 0.5 mm in scan direction.

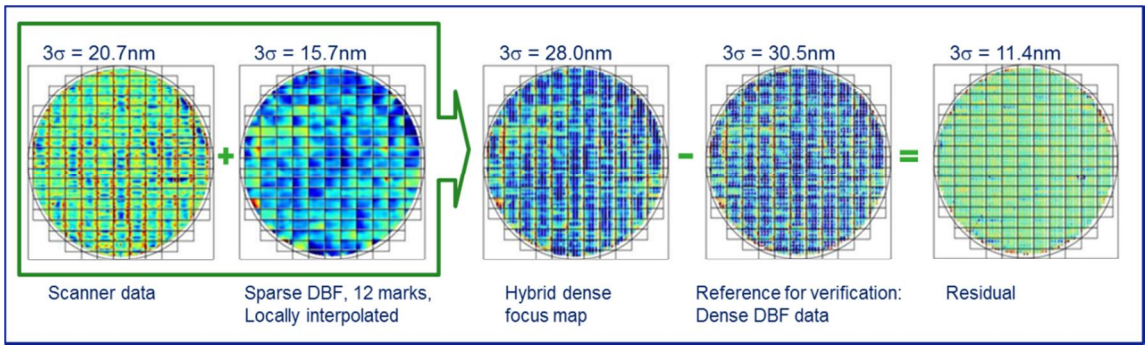

Figure 3: Example of hybrid dense focus map generation and validation against dense DFM measurements. All plots have the same color scale.

Figure 3 also compares the HDFM against the focus map from densely measured DFM data from the same wafer; both maps are visually almost indistinguishable and show essentially the same overall variation. The difference between the two dense maps shows a 3-sigma variation of the residual differences that is well within the expected TFMU (total focus measurement uncertainty) of the DBF targets. [9] The residual map also indicates that the largest differences are confined to the very outer-most measurement points on incomplete exposure fields, where applying suitable constraints to the tilt fit could likely further improve the result. The comparison clearly shows that there is a good correlation between the higher spatial frequency scanner data and on-wafer focus measurements, and hence the value of the scanner contributions to the overall estimation of focus error distributions across a wafer.

This conclusion is further confirmed by the comparison in Fig. 4, where we assess the impact of different local focus estimates on the measured CD distributions of a focus sensitive feature. The measurements are done on a small monitoring module that contains line-space (L/S) patterns at a few different pitches that are suitable for CD measurements with either YieldStar or CD-SEM. The module also contains DBF targets in immediate vicinity, i.e. within 500 um of the L/S targets. The modules are located at the left and right side of the SN2 layout and are repeated 27 times in scan direction, providing 54 samples of CD and focus measurements for every exposure field. The CD data shown here are from a semi-isolated feature at 380 nm pitch, drawn line width 92 nm, which is very focus sensitive. Measurements are done using the YieldStar CD metrology capability for both horizontal (plotted in green) and vertical (plotted in blue) line orientations through focus on a FEM (focus exposure matrix) wafer.[2]

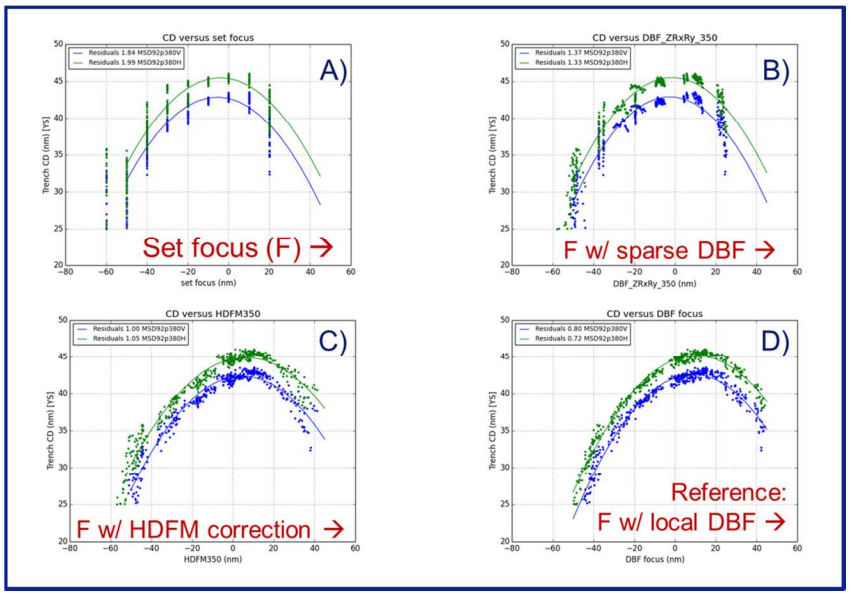

Figure 4: Impact of local focus estimates on distribution of measured CD data from 54 intrafield locations. A) CD versus scanner focus setting per field; B) CD versus local focus estimates from sparse DBF measurements; C) CD versus local focus from DBF and scanner data (HDFM); D) CD versus focus from dense DBF measurements.

Figure 4A shows the measured CD values through "set" focus. "Set focus" is the input to the scanner exposure recipe, at focus offset steps of 10 nm. With increasing defocus in either direction there is significant increase of CD variations, for both H and V oriented lines. It is of course possible to determine an average CD value per focus value, and to fit a Bossung curve to the data, as indicated here by a simple 2nd order polynomial fit. However, if we consider local focus variations, it becomes clear that a large part of the apparent CD variations are correlated to these focus values. For reference, Fig.4D plots the CD measurements against focus measurements from DBF data sampled in immediate vicinity of the CD targets. The comparison clearly suggests that a significant contribution to the CD variation in 4A is related to focus variations, which become more significant in terms of CD impact at off-focus conditions. After considering the local focus condition on wafer, as measured by DBF, the CD data clearly fall much closer overall to the expected Bossunk-like through-focus behavior. The remaining CD variation seems not much dependent on defocus, suggesting that it is mostly related to non-focus related variability. We conclude that the DBF measurements can provide a good prediction capability of focus-related on-wafer printing performance.

While it is not practical to place a DBF target in the vicinity of every focus sensitive product pattern, comparison between Fig.4C and 4D suggests that our proposed method of HDFM generation from sparse DBF and dense scanner data should provide very comparable performance in terms of local focus estimates, and consequently pattern defect probability estimates. Fig. 4B, using linear fitting of sparse DBF data only, shows significant improvement over the "set" focus baseline, but adding scanner data into the HDFM provides another significant improvement towards predicting on-wafer printing performance for focus sensitive patterns.

We conclude that the HDFM approach should be appropriate and well-suited for our goal of local defect prediction. Possible extensions of the concept, to account for more product/process dependent variations that we see in the experiments at IMEC will be discussed in Ref.8, where inclusion of additional metrology data and modeling of additional topography effects from gds layout data are considered.

3.2 Verification of defect mechanisms

We collected and reviewed a very large number of SEM images at hotspot and defect locations that were identified by PWQ and LMC simulations. All data shown here are in resist (ADI). The first step in verifying where exactly patterns start to fail, i.e. in determining defect mechanisms is extensive visual review of the SEM images and comparison between measured contours and simulations, in order to assess the validity of the LMC model predictions. Figure 5 shows one example for a hotspot location that was initially identified by a PWQ experiment using a bright field inspection tool and repeater analysis.

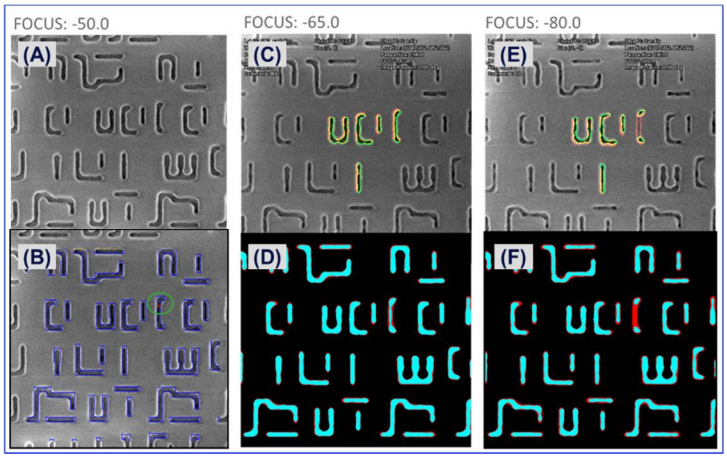

Figure 5: Comparison of SEM images against simulation through focus for one hotspot location. A,B) focus = -50nm; B) SEM image overlaid with design layout and LMC defect marker. C,E) SEM images at larger defocus, with extracted contour from best focus (red, for reference) and defocus condition (yellow); D,F) simulated contours at BF (red) and defocus (cyan), corresponding to C and E.

The image at focus setting of -50 nm corresponds to the edge of the process window, where first defects are being flagged by the bright field inspection tool in PWQ. From a single SEM image alone (A), it would be challenging to determine where exactly the defect occurs and what the defect mechanism is. However, model-based process window analysis identifies one specific location where the simulation predicts the most severe pinching of the starts occurring – Fig.5B overlays the SEM image with the drawn target layout and the defect marker (in red) from the LMC analysis, where pinching (aka necking) of the resist contours below 35 nm is being flagged. Going further out of focus, the actual defect becomes more visible, although it becomes an obvious catastrophic pattern failure only far outside the PW boundary. For better visualization, the model results in Fig. 5 D and F show contours at best focus (BF) in red, overlaid with defocus simulations in cyan. Figure 5 C and E show corresponding SEM images overlaid with the extracted contours, where red are reference contours at best focus and yellow contours are at defocus.

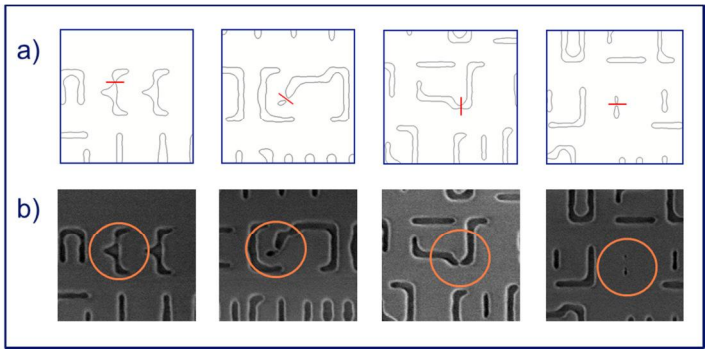

Figure 6: Examples of additional hotspot patterns and defect mechanisms that were identified by model prediction (a) and verified by SEM review (b).

We generally see very good qualitative agreement between the SEM images we reviewed and the model predictions, in particular with respect to the specific locations where the worst pinching or line end pull-back are seen, which are the dominant defect mechanisms for this layout. A few more examples are illustrated in Fig. 6. Our conclusion is that all defect types predicted by the model can be recognized in the SEM images. We also did not encounter any hotspot/defect types identified through PWQ that were missed by the model based approach.

3.3 Quantification of defect occurrence

While visual review of SEM images is quite effective, it cannot be used for quantitative analysis. A quantitative definition of when and where a critical pattern becomes a defect is needed, which would allow automated defect verification and dispositioning. The well-known CD based criteria, e.g. defining 10% CD change as defect are straightforward in principle, but CD measurements are challenging in practice for complex 2D patterns such as in Fig.6.

We are considering several alternatives in terms of measurement tools and analysis methods. This is work in progress and we limit the scope of this paper to giving examples only.

As we collected several thousand review SEM images, we apply image processing for data analysis, starting with contour extraction, as already shown in Fig.5. We use this approach in the following sections, based on local contour area estimation from calculating the number of image pixels within a particular pattern shape. It would be quite difficult to detect localized necking defects from contour area of the entire image, however by limiting the data extraction to the immediate vicinity of the predicted defect coordinates, e.g. to a single polygon we are able to extract a usable signal. (see Section 3.4)

Another approach is usage of an e-beam inspection tool (EBI), which offers both die-to-die and die-to-database inspection capabilities.[11] For the latter, the tool offers various detection modes that compare the measured image to the target design. This is very similar, in principle, to the model-based 'virtual inspection' in LMC, so we expect that detection thresholds between defect prediction and inspection can be jointly matched towards a sensitivity that also agrees with impact on device performance. First tests were performed at Hermes Microvision (HMI) using a using eP3 XP tool together with HMI's Supernova2.0 data analysis system (same naming as IMEC's test vehicle is coincidental), on a wafer exposed at IMEC. Hotspot locations and care areas are determined from LMC and sent to the EBI tool together with layout data for localized inspection. A first example is shown in Fig.7 where measurements through focus on a FEM wafer are used for a defect-based DOF estimation.

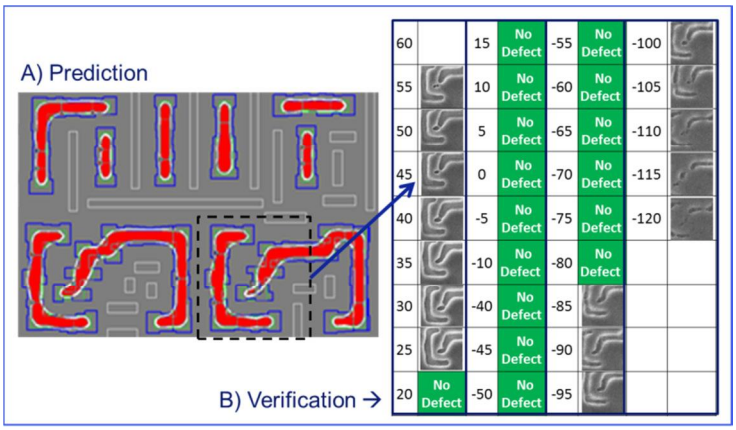

Figure 7: Example of die-to-database inspection for defect verification on an EBI tool: local inspection region is defined around predicted defect (A), inspected through focus on a FEM wafer (B).

We are also evaluating usage of a CD-SEM tool and contour extraction. Hitachi recently reported contour extraction capabilities that are consistent with and well-matched to CD measurements on the same tool.[12] This appears attractive in terms of matching defect metrology and litho model, since the latter is generally calibrated against extensive CD-SEM measurements. Several analysis methods can be applied to the extracted contours, such as contour shape analysis, comparison against target layout or reference data. A first example, as proof of concept, is illustrated in Fig.8, where we compare CDSEM contours against simulation. For quantitative evaluation, we apply the same LMC detector – a check for contour necking– to both simulated and measured contours. The ability to use exactly the same metrics on simulation and experimental data is another promising aspect of this approach.

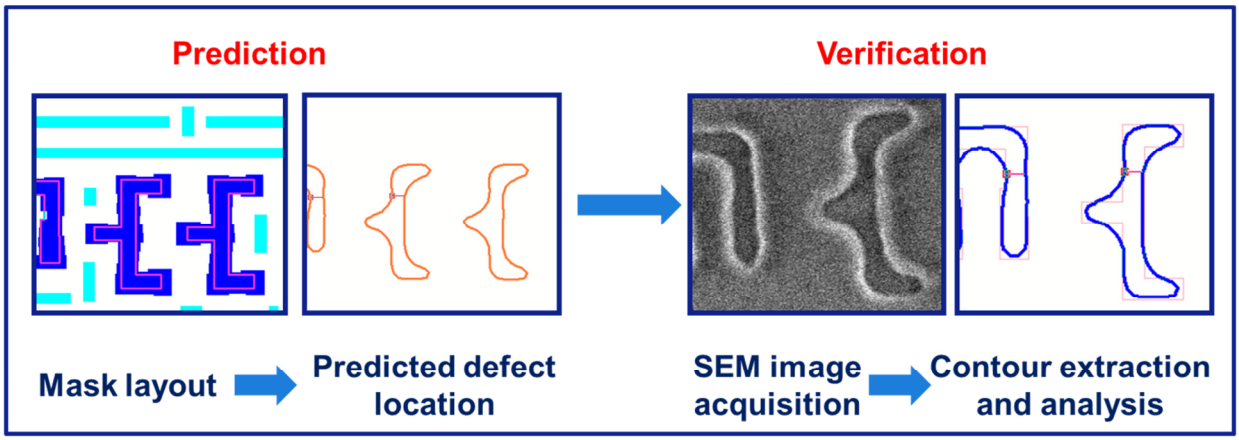

Figure 8: Usage of contours extracted from CD-SEM images for defect verification. LMC necking (NK) detector is being applied to simulated (Prediction) and SEM contours (Verification), respectively.

A common requirement for the desired defect verification method is the ability to measure at any arbitrary location on a wafer in order to enable on-product hotspot monitoring. This capability has been established for the methods considered. Another commonality is that all the analysis methods considered will benefit from knowing the exact location of the expected defect.

3.4 Full-wafer defect prediction & verification

A quantitative distinction between defects and non-defects needs to be established for analysis and statistical interpretation of wafer data in terms of defect counts, defect probabilities and related quantities. For the following analysis we use image processing of SEM images to estimate contour area of individual pattern features, as illustrated in Fig. 9. In this we utilize our understanding of the actual defect mechanism for each hotspot, which we qualitatively established in Section 3.2. Specifically for the location shown in Fig.9A, we established through simulation and SEM review that the highlighted small trench pattern shows the fastest degradation with defocus, and will eventually become a catastrophic defect. The images are at varying focus setting on a FEM wafer. The numbers shown are the area estimates for the specific defect pattern, in nm^2.

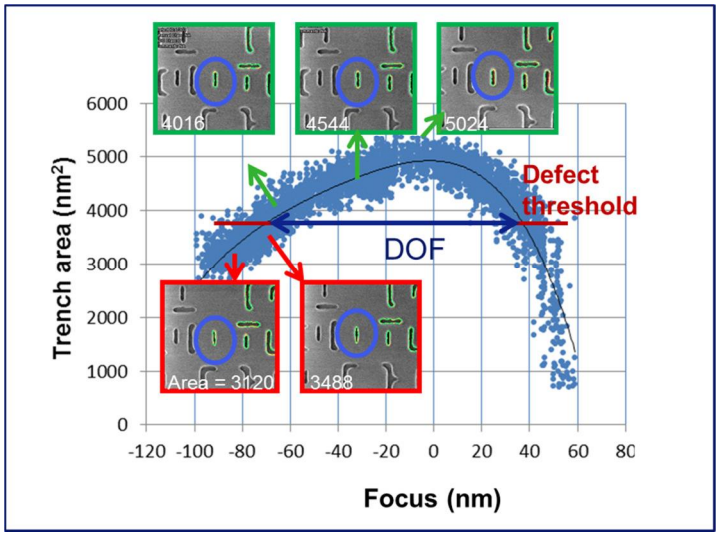

Figure 9: Semi-automated quantitative analysis based on image contour extraction.

Our initial defect definition is based on 'expert review' of a subset of available SEM images and subjective decision between defect and non-defect, leading to a pattern area threshold estimate of 4000 nm^2. This value also corresponds to 20% reduction from the peak measurement, which seems reasonable for this specific pattern, if 10% CD reduction in 2 dimensions is considered. Figure 9B plots area measurements from 6000 individual hotspot images, taken over 32 focus modulations on a FEM wafer, with 175 samples of the same hotspot pattern across the entire exposure field. The high throughput of the review SEM allows generation of large data sets, which will be advantageous for statistical data analysis. The area values are plotted against local focus estimate from the HDFM (see Sec. 3.1). Due to the focus variations across the wafer, every data point essentially corresponds to a different focus value. Every data point is from one single SEM image. Obviously there is significant noise on the data, but overall it shows a Bossung-like trend through focus that can be well fitted by a 4^{th} order polynomial.

With this, we can translate the defect threshold in contour area into a defect threshold in terms of defocus values, and correspondingly DOF and possibly BF shifts. The focus thresholds establish a simple defect prediction model with respect to the HDFM values: at focus values outside the DOF the hotspot is expected to become an actual defect on wafer, inside the DOF range it is expected to still print to specs. To account for the statistics, i.e. process variations other than focus, and signal noise, we can also determine defect probability by a logistic regression fit to the data once wafer data is available. In principle this can be done for every hotspot type.A direct, quantitative comparison of the LMC model predictions to the contour area is not straightforward, primarily because the model is calibrated against CD measurements from a different SEM tool. However, if we allow for some scaling of the data, we can get reasonably good agreement of the through-focus variation. More importantly, as shown in Fig. 10, we see a very good correlation between predicted and measured DOF for various hotspot locations. As illustrated four different placements of the same target geometry are considered here. The drawn dimensions of the small trench patterns are identical, however the surrounding patterns are different, while overall pattern density appears similar, and from subjective judgment all locations look somewhat semi-isolated. However the available DOF varies by up to 30nm between the most and least critical location. Very importantly, arguably more important than prediction of absolute CD, the model correctly predicts which location is the most focus sensitive.

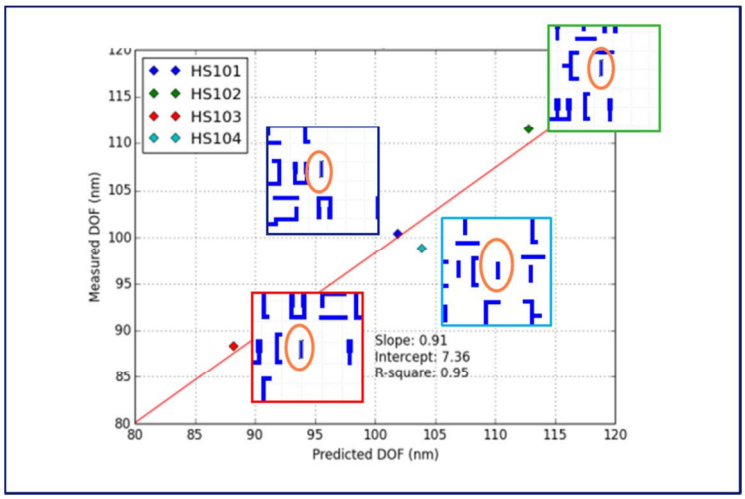

Figure 10: Ranking of representative device patterns by depth-of –focus (DOF). Good match between simulation and wafer data, and correct identification of DOF limiting pattern.

For an actual hotspot monitoring application, the most limiting pattern locations could be chosen with preference and measured primarily at locations with predicted high defect probability, instead of the uniform sampling from a FEM wafer used to generate Fig.9.

Figure 11 shows the result of defect prediction and verification for the most DOI limiting pattern as shown above (HS103). The wafer was exposed with some uniform offset from best focus to emulate a situation where available DOF is comparable to the actual range of focus variations, and to induce a larger defect count for illustration. In order to reduce false positives due to process variability or other than focus and noise, we allow for an additional margin outside the estimated DOF limit. In other words, prediction and sampling for verification are directed towards locations with largest focus excursions and highest expected defect probability.

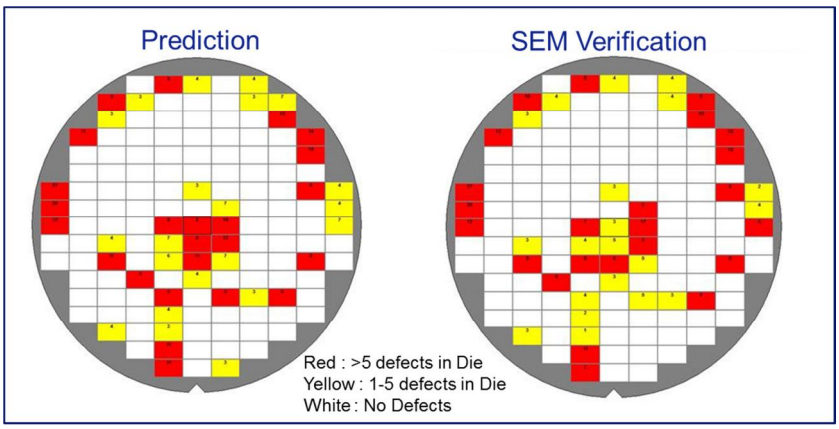

Figure 11: Wafer maps from defect prediction and verification. Wafer was exposed with uniform focus offset to increase defect count for proof of concept. Color coding is by defect count per die as indicated

The comparison between prediction and wafer measurements at the predicted locations shows good agreement between prediction and verification, in spatial distribution across the wafer as well as total defect count.

Finally, we extend our data analysis to more complex patterns of interest, following the same principles and methods as discussed above. Data analysis is again based on contour extraction and area local estimation in the vicinity of the known necking locations on the more complex target polygons. This approach might be expected to be less robust for

larger features than for the small trench patterns studied before. Nevertheless we find comparable results for a multitude of pattern types. In Fig.12 we present a comparison across different hotspots in terms of capture and nuisance rates (CR, NR) that we define as following. CR: number of correct predictions normalized by total number of verified defects. NR: number of false positives normalized by total number of predicted defects. The magnitude of these numbers will depend significantly on the noise level on the wafer data as well as on the data sampling and distribution of focus variations. We also note that the defect prediction for this analysis is based entirely on LMC results, using a single detector (necking) with the same threshold setting for the entire layout.

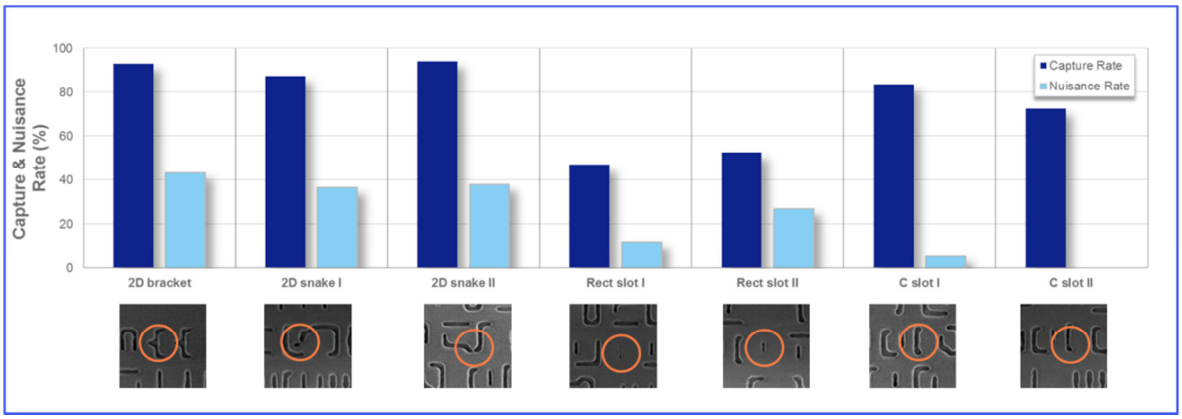

Figure 12: defect prediction capability in terms of capture and nuisance rates for multiple hotspot types.

4. CONCLUSIONS

We extend a holistic lithography framework towards prediction, detection and verification of on-products patterning defects. Hotspots, i.e. process window limiting patterns are identified by computational lithography, and characterized by available depth of focus (DOF). The locations of the hotspots and overall PW are mapped locally across the layout of the mask. Prediction of where a hotspot becomes a defect on wafer is made possible by generating a map of local focus variation over the entire wafer. This map is constructed from sparse, focus sensitive scatterometry measurements and dense data from the scanner's leveling system. Locations where the focus variations exceed the available DOF are flagged as potential defect locations, and verified by SEM metrology.

Our experimental study on a 10nm BEOL metal layer process shows good accuracy of the computational model for prediction of the critical failure mechanisms, in estimating the correct DOF for the critical patterns, and therefore in locating the most critical PW limiters. We established a SEM data analysis flow that allows verification of actual versus predicted defects by establishing quantitative defect criteria. The effectiveness of the algorithm relies on exact knowledge of defect mechanisms within the layout in order to enable local image analysis.

With these components we implemented a proof-of-concept data flow for full-wafer defect prediction and verification, and exercise this experimentally. The results currently show good agreement in terms of total defect count and encouraging results in terms of capture and nuisance rates. Ongoing work will address inclusion of scanner control for defect reduction, as well as inclusion of additional data sources and parameters for added accuracy.

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